AB4518

Interfacing to the VP5311/VP5511 Video Encoder

Application Note

AB4518 - 1.4 August 1996

INTRODUCTION

All references in this document to VP5311 equally apply to the VP5511. Interfacing the video encoder in a complex digital video system requires an understanding of how the encoder synchronizes itself to the rest of the system. The VP5311 simplifies the digital to analog interface by integrating the whole composite encoding function in a single chip. Only a small number of external components are required. It is the digital system interface, however, that has several different implementations depending on the particular system requirements. The purpose of this application note is to describe the different interfacing options on the VP5311 as well as describe the genlock and closed captioning features.

SYSTEM DATA FLOW AND SYNCHRONIZATION

In a typical video system, such as a cable or satellite set top box, there are two sources of video information. One is digital and consists of the primary source of programming material. The other is analog and is sourced by on screen display-OSD, PIP tuner, external antennae, or other analog overlay sources. To control the synchronization of these sources to the actual television receiver a master/slave arrangement is required. Analog video arrives asynchronously with respect to the digital video data, and they both need to be properly synchronized with respect to the NTSC/PAL timing requirements of the receiver. The master/slave synchronization is handled between the video encoder and the MPEG-2 decoder. The VP5311 can work in either master or slave mode to enable it to interface to all MPEG decoders including master or slave only mode decoders.

The driving factor forcing this synchronization are the timing requirements of NTSC and PAL television receivers. In these receivers, synchronization signals in the video source material control the vertical and horizontal timing. There are a precise number of these signals and their timing requirements are very strict to allow compatibility with a wide variety of sources and backwards compatibility with millions of televisions purchased over several decades. In addition to the horizontal and vertical synchronization, colour televisions require a colour burst signal immediately following the horizontal sync. This is a 9 cycle sinusoid of a specific frequency. The receiver needs to phase and frequency lock to this signal in order to properly extract colour hue and saturation information from the video signal source.

SLAVE MODE INTERFACE

A video output subsystem is shown below in Fig.1. In this mode, the MPEG-2 Video Decoder is the master while the VP5311 VEC slaves to it.

In this system PIP, OSD, or analog video from an external source can be overlaid on the digital video source. This is inserted and controlled through a switch on the output of the VP5311 and it's filters. Genlock (the process of synchronising Hs, Vs and the colour sub-carrier) can only be achieved, when the video encoder is in slave mode. In this mode the MPEG-2 decoder synchronizes the HS and VS of the digital video to the analog source and it then outputs the digital video with the embedded TRS (Timing Reference Signals) codes. These codes contain blanking information, field identification, and active video synchronization which is inserted prior to the beginning of the active video line data, corresponding to CCIR Rec 656. This data stream has the formats shown in Fig.2.

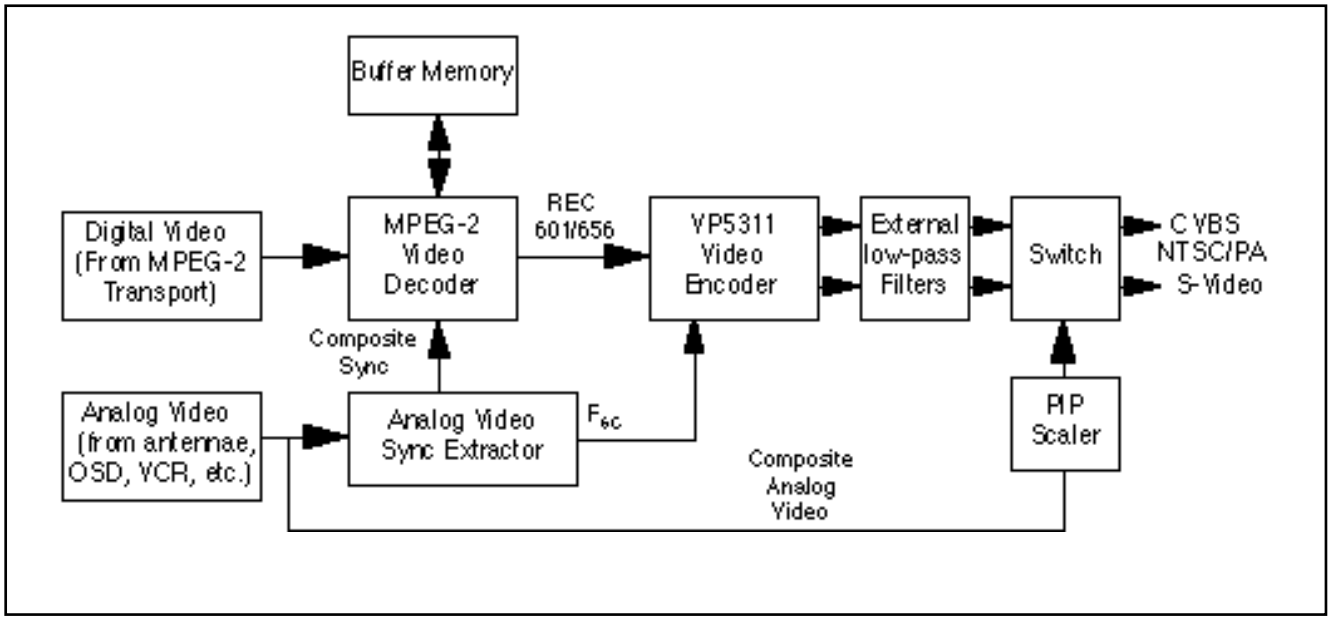
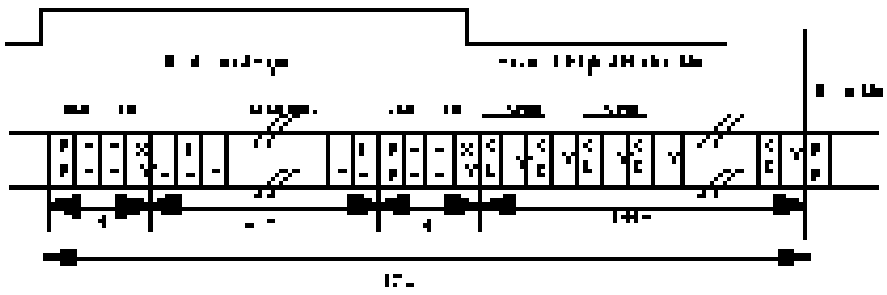


Fig.1 Video Encoder Slave Interface



The XY byte in the EAV and SAV codes has the following bit definitions:

1	F	V	H	P_3	P_2	P_1	P_0

F = 0 during field 1
1 during field 2

V = 0 outside field blanking
1 indicates that this is a field blanking period

H = 0 in SAV (Start of Active Video)
1 in EAV (End of Active Video)

P_3, P_2, P_1, P_0 are protection bits that depend on the states of the previous 3 bits. There function is to allow the correction of 1 bit errors and detection of 2 bit errors.

Fig.2 CCIR Recommendation 656 Data Format for 625/50 system

The REC 656 data consists of 1728 8-bit samples per line for PAL systems while the NTSC system has 1716 samples per line. Each system has 1440 active video samples, while PAL has 12 more blanking codes to give it a total of 1728 samples. The video encoder receives this information at 27 MHz through an 8-bit port. As it receives data, the EAV and SAV codes are decoded and the appropriate digital synchronization signals and field specific colour subcarrier phase (either 0° or 180°) are generated. The active video consists of alternating luma samples separated by either a C_b or C_r sample. It can be seen that there will be 720 luma samples per line while there will be 360 chroma pairs per line. The chroma pairs will be combined with every other luma sample to form a co-sited sample. CCIR REC 656 specifies a 27 MHz sample clock rate, which means the luma data rate is 13.5 MHz, while each chroma sample has a 6.75 MHz rate. Fig. 3 below shows the block diagram of the VP5311:

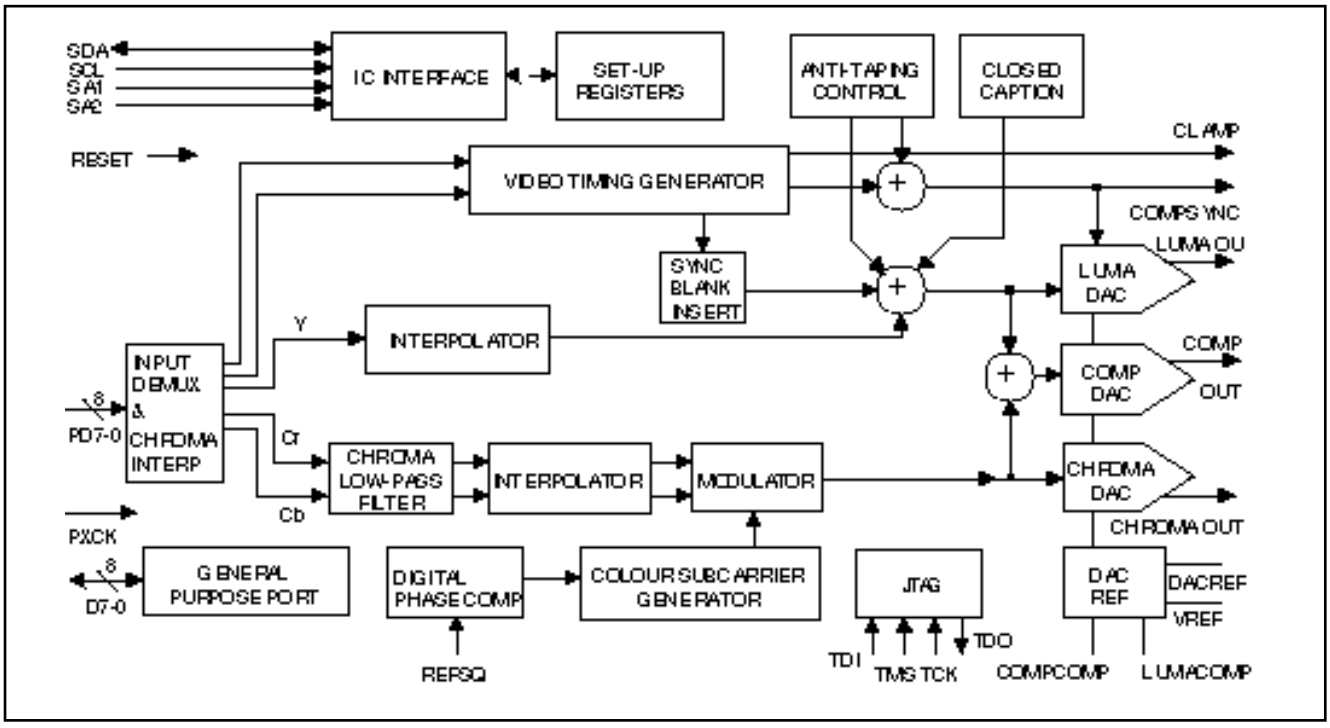


Fig.3 Block diagram of the VP5311

As the VP5311 receives the active video, the chroma samples are filtered and interpolated up to a 27 MHz rate where they are modulated together at the colour sub-carrier frequency, F_{sc}. The luma samples are also interpolated up to 27 MHz. The interpolation process for both the luma and chroma paths are quite simple. The algorithm takes two samples, averages them and then inserts the result between the two original samples. The end result of the interpolation process is that the output rate is doubled from the nominal 13.5 MHz, to 27 MHz. This helps to minimize the sinx/x distortion and quantizing noise that is inherent in digital sampling. After interpolation, the luma samples are combined with the synchronization signals coming from the video timing generator. The luma and chroma data is then converted to analog through three 9-bit DACs. Two DACs are used for S-Video applications where the luma and chroma are separate. The 3rd DAC is used for composite video where the luma and chroma data are numerically summed prior to being converted.

MASTER MODE INTERFACE

The previous example showed the VP5311 operating as a slave to the MPEG-2 decoder. Other systems require the video encoder to operate as the master to control data flow from the MPEG-2 decoder's buffer to the output video monitor. In Master Mode, the video encoder generates HS/VS/FC outputs, that connect to the MPEG-2 decoder. When the decoder receives the Hrizontal Sync control signal, it then outputs the field after a short delay. The synchronization between the MPEG-2 decoder and the VP5311 is critical as the television receiver is expecting a steady stream of video along with the precise sync signals that are embedded in it. This is illustrated in Fig.4.

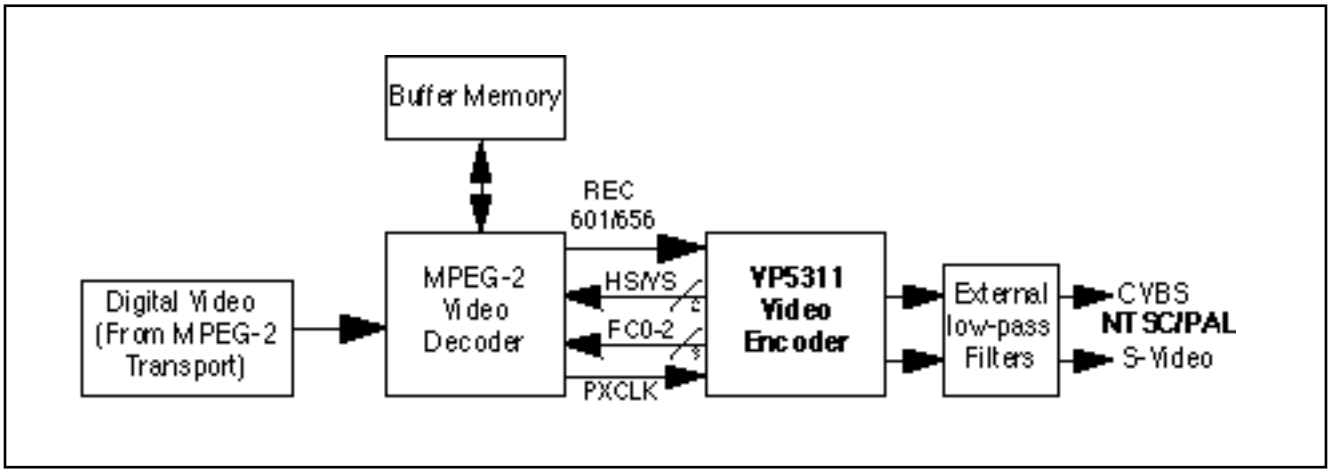


Fig.4 VP5311 Master showing Master Mode Signals

To configure the VP5311 for master mode the TRSEL bit in the GPSCTL register must be set to a '1'. Once in this mode, the GPP (General Purpose Port) is automatically configured to produce the following outputs:

Pin Number	Function
3	VS
4	HS
5	FC0
6	FC1
7	FC2

VS is the start of the field sync datum, in the middle of the equalisation pulses.

HS is the line sync which is used by the preceding MPEG2 decoder to define when to output digital video data to the VP5311.

FC0 - 2 are the field count outputs, defined in the table below:

FC2	FC1	FC0	Field
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Note that only fields 1 - 4 are used in NTSC, so FC2 is not used. In PAL fields 1-8 are used.

The VP5311 asserts the HS signal a certain time prior to the time that the television receiver actually requires a particular line of video. This is because there is an inherent delay through the video encoder and the MPEG decoder. The delay through the MPEG decoder is known as the pipeline delay and will be different with each manufacturer's MPEG decoder. To accommodate this delay, the VP5311 can be programmed to advance the timing offset of the HS pulse it presents to the MPEG decoder. This is illustrated in Figure 5 below. The programmed value is a number that represents the number of 13.5 MHz pixel clocks between the time the HS pulse goes active to the time that the decoder puts the first sample on the bus.

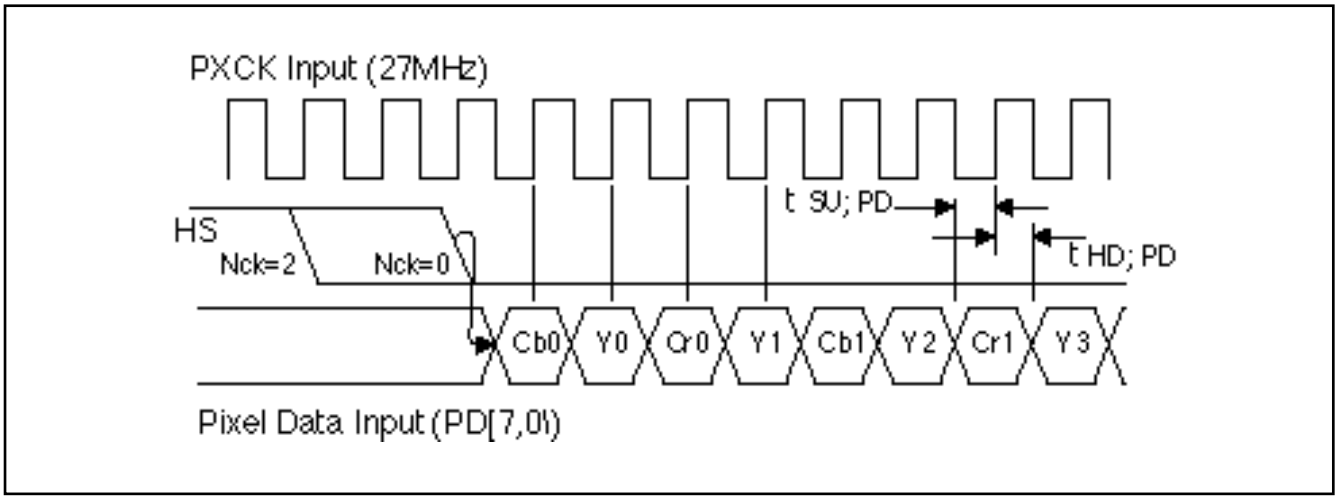


Fig.5 REC 656 interface with HS output timing

PROGRAMMING HS OFFSET

The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see Figure 5. This is done by programming a 10 bit number called HSOFF into the HSOFFM and HSOFFL registers, HSOFFM being the most significant two bits and HSOFFL the least significant eight bits. A default value of 07EH is held in the registers.

The value to program into HSOFF can be looked up in the table below:

For NTSC and PAL-M:

NCK	HSOFF	Comment
0 to 120	126 to 6	HS normal (64 cks)
121 to 138	863 to 801	HS pulse shortened*
184 to 857	800 to 127	HS normal (64 cks)

For PAL-B, G, H, I, N:

NCK	HSOFF	Comment
0 to 131	137 to 6	HS normal (64 cks)
132 to 194	869 to 807	HS pulse shortened*
195 to 863	806 to 138	HS normal (64 cks)

*HS pulse shortened means that the width of the pulse will be less than the normal 64 13.5MHz clock cycles.

Where Nck = number of 13.5MHz clock cycles between the falling edge of HS and Cb0 (first data I/P on PD7-0), see Figure 5. Decreasing HSOFF advances the HS pulse, (numbers are in decimal).

The interruption in the sequence of HSOFF values is because the HS signal is jumping across a line boundary to the previous line as the offset is increased. The register default value is 7EH, and this sets Nck to 0, ie. the HS negative edge and Cb0 are co-incident in NTSC mode.

Example 1, if an offset of eight 13.5MHz clock cycles is required (pipeline delay of 592.6ns) then:

HSOFF = 126 - 8 = 118 (76H) for NTSC

HSOFF = 137 - 8 = 129 (81H) for PAL

Example 2, if an offset of 300 13.5MHz clock cycles is required (pipeline delay of 22.222us) then:

HSOFF = 800 + 184 - 300 = 684 (2ACH) for NTSC

HSOFF = 806 + 195 - 300 = 701 (2BDH) for PAL

GENLOCK

When combining video from different sources, the Horizontal Sync, Vertical Sync. and colour sub-carrier phase need to be synchronized, as shown below:

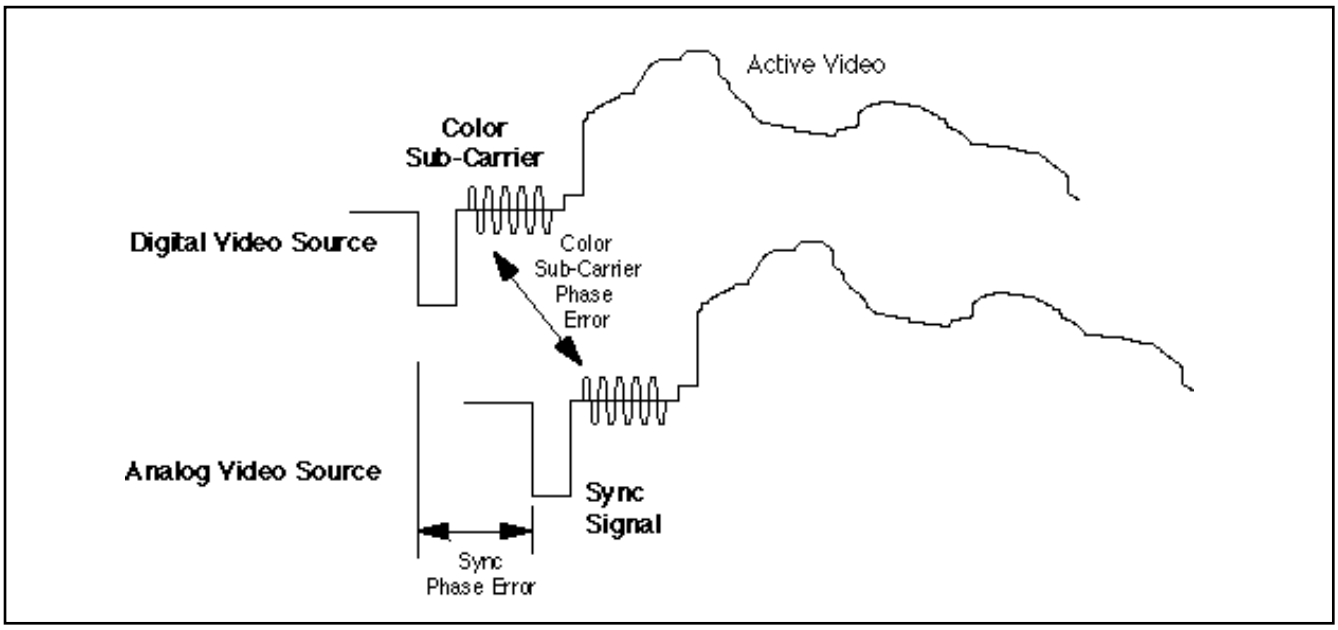


Fig.6 Synchronization Phase Errors

The process of synchronizing Horizontal Sync (HS), Vertical Sync (VS), and the colour sub-carrier is known as Genlock. Synchronizing HS and VS is required so that the analog video overlay is properly positioned on top of the video originating from the digital video source. For this process, the genlock circuit needs to remove the synchronization phase errors.

Obtaining colour sub-carrier synchronization is required for a very different reason. In Figure 6 above it implies that by removing HS and VS phase errors, the colour sub-carrier synchronization would occur by default. However, the colour sub-carrier phase from two different sources can vary significantly. The video receiver aligns its colour sub-carrier phase to the colour burst signal of the incoming video. No colour hue and saturation information would be present, if the receiver were phase locked to the colour burst of the digital source, and the information being displayed was from the analog source. Thus, colour sub-carrier genlock is required to maintain hue and saturation accuracy when video information is being displayed from one source while the video receiver is synchronized to the colour sub-carrier of another.

VP5311 GENLOCK

The VP5311 implements colour sub-carrier genlock. It requires the use of an external circuit that extracts the synchronization signals as well as providing a colour sub-carrier signal, as indicated in Figure 7. This signal is a continuous square wave that is phase locked to the colour sub-carrier of the incoming analog video signal. Horizontal and Vertical Sync genlock must be performed in a separate circuit, the MPEG-2 decoder being the logical location. There are several different circuits that perform this HS/VS sync extraction and colour sub-carrier generation.

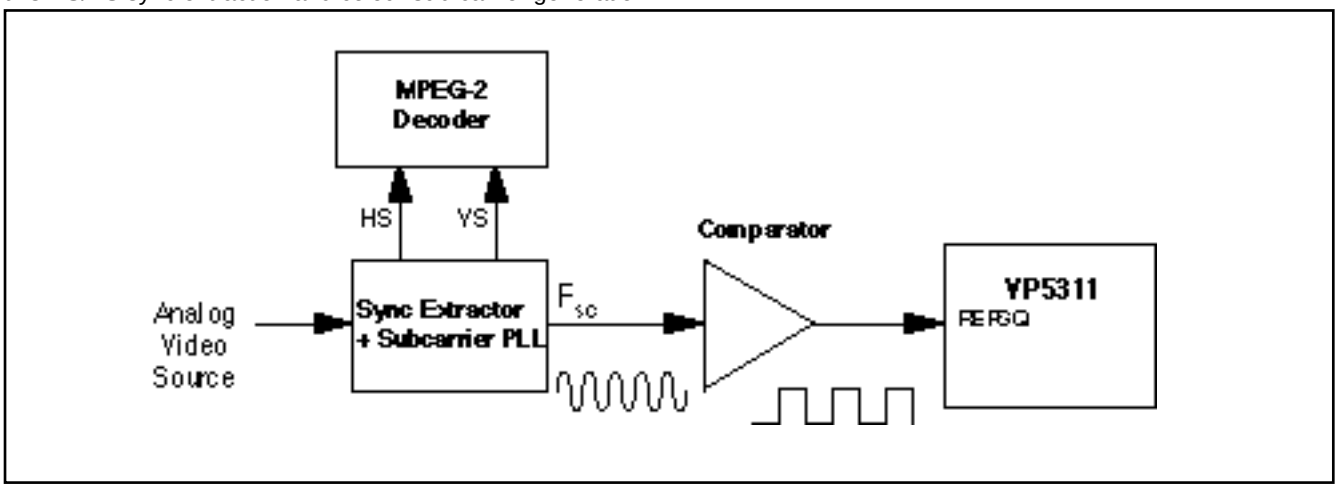


Fig.7 Generic Colour Sub-Carrier extracror

When genlocking to an external analog source, the digital source needs to slave to the analog signal. As analog video arrives asynchronously, the MPEG decoder must be synchronised to the extracted analog HS & VS signals, Fig.7. The MPEG decoder will then generate a REC656 data stream with the embedded synchronisation bytes and the VP5311 locks to these in slave mode, effectively locking to the analog source.

The subcarrier is recovered from the analog source and converted to a digital level signal and then input to the REFSQ pin. A digital phase locked loop, in the VP5311, then locks its own internally generated subcarrier to the incoming square wave. Once genlock has been achieved the digital signal can be overlaid on top of the analog one (or vice versa), this is useful for OSDs, PIP etc..

This sync extractor and subcarrier PLL circuit can use a variety of video decoder products presently available. Several of these are low-cost for use in high volume, consumer TV markets; some devices combine HS and VS into a composite sync which may need to be separated externally. The colour-subcarrier signal will be a continuous frequency (particular to NSTC or PAL system) and phase aligned to the colour sub-carrier of the source. Since this is a sinusoidal signal and the VP5311 expects a digital square wave, a squaring function needs to be implemented. A comparator with TTL output operation would fulfil this function. The VP5311 will then phase lock its colour subcarrier generator to that of the external analog source.

CLOSED CAPTIONING

Introduction

The VP5311 has the facility to generate closed caption data on line 21, as used on NTSC systems in the USA. Closed captions are used as a means of subtitling programs to assist people with poor hearing or for an alternative language to the audio channel. Full screen format text can also be sent and displayed.

The data to be displayed needs to be sent over the I^2C bus to the VP5311 and this document describes how this software should operate.

Closed Caption System

This is specified in the EIA-608 Line 21 Data Services for NTSC and should be referred to for further information. Field 1 is used for normal caption service while field 2 tends to be reserved for special use such as a second language.

Two bytes of data are coded on the line 21 of each field, see Figure 8, below. The data is coded as NRZ data with odd parity after a clock run-in and framing code. The clock run-in frequency = 0.5034965MHz which is related to the nominal line period, D = H / 32 or D = 63.55555556 / 32µs.

Two types of data are sent, printing and non-printing characters. The latter are two byte pairs that are transmitted twice on successive frames and are used for control purposes, such as the display position. Printing characters are text to be displayed on the screen; generally ASCII code is used with odd parity in the MSB, but there are some other codes for special and non-English characters.

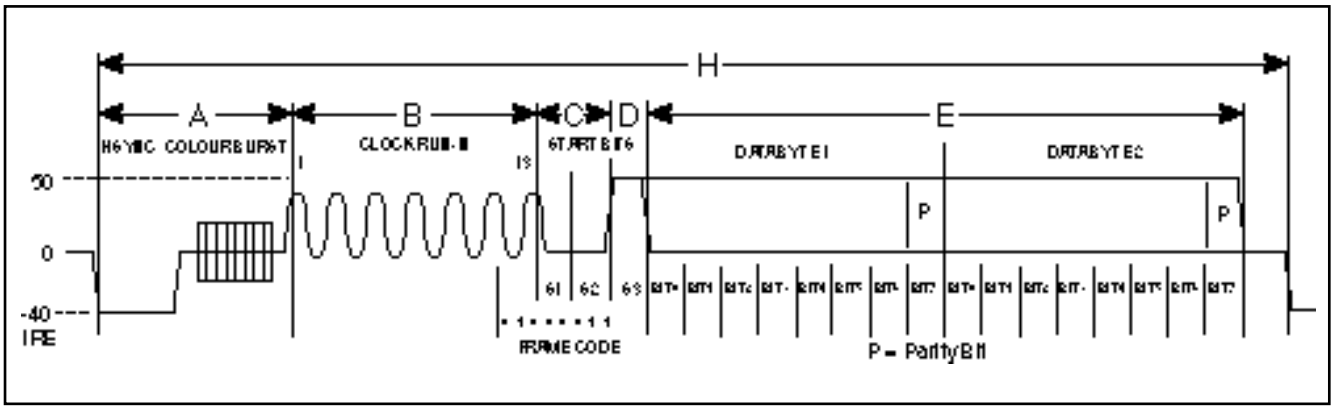


Fig.8 Closed Caption format

Interval	Description	Encoder minimum	Encoder nominal	Encoder maximum
A	H-sync to clock run-in	10.250µs	10.500µs	10.750µs
B	Clock run-in [2, 3]		6.5D (12.910µs)	
C	Clock run-in to third start bit [3]		2.0D (3.972µs)	
D	Data bit [1, 3]		1.0D (1.986µs)	
E	Data characters [4]		16.0D (31.778µs)	
H	Horizontal line [1]		32.0D (63.556)	
	Rise / fall time of data bit transitions [5]		0.240µs	0.288µs
	Data bit high (logic level one) [6] Clock run-in maximum	48 IRE	50 IRE	52 IRE
	Data bit low (logic level zero) [6] Clock run-in minimum	0 IRE	0 IRE	2 IRE
	Data bit differential (high - low) Clock run-in differential (max. - min)	48 IRE	50 IRE	52 IRE

Notes
1. The Horizontal line frequency f_H is nominally 15734.26Hz ±0.05Hz. Interval D shall be adjusted to D = 1/(f_H x 32) for the instantaneous f_H at line 21.
2. The clock run-in signal consists of 7.0 cycles of a 0.5034965MHz (1/D) sine wave when measured from the leading to trailing 0 IRE points. The sine wave is to be symmetrical about the 25 IRE level.
3. The negative going midpoints (half amplitude) of the clock run-in shall be coherent with the midpoints (half amplitude) of the Start and Data bit transitions.
4. Two characters, each consisting of 7 data bits and 1 odd parity bit.
5. 2 T Bar, measured between the 10% and 90% amplitude points.
6. The clock run-in maximum level shall not differ from the data bit high level by more than ±1 IRE. The clock run-in minimum level shall not differ from the data bit low level by more than ±1 IRE.

DESCRIPTION OF VP5311 OPERATION

Five registers are used in the VP5311 for closed caption, four to store the data to be transmitted (**CCREG1 - 4**) and one to control the operation (**CCTL**). These are detailed below:

Address	Reg Name	Description
F0	**CCREG1**	1st byte to be encoded onto line 21, field 1
F1	**CCREG2**	2nd byte to be encoded onto line 21, field 1
F2	**CCREG3**	1st byte to be encoded onto line 21, field 2
F3	**CCREG4**	2nd byte to be encoded onto line 21, field 2

Note in the above 4 registers the MSB is ignored, this is the parity bit automatically added by the VP5311, odd parity is used.

F4		**CCTL**		1st byte to be encoded onto line 21, field 1				
bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	F2EN	F1EN

Only two bits are contained in the **CCTL** register, F1EN enables closed captioning onto line 21 field 1, F2EN is the same but for field 2. By default both bits are at '0' disabling closed captioning.

When a byte is received into a **CCREG** register it is encoded on the next available field, the registers are then set to the null byte (80H). Null bytes are ignored by the decoder (except for non-printing characters, see above), so gaps in the transmission of characters do not matter as long as these are filled with null characters. The 7 cycles of clock run-in and the odd parity bits are automatically added by the VP5311 before transmission.

Software Operation

Normally at initialisation the F1EN bit from reg **CCTL** is set to a '1' to enable closed caption on line 21 field 1. If encoding on line 21 field 2 is required the F2EN bit is set (both can be set if desired).

Two or four characters are programmed into the **CCREG**s for transmission. To ensure correct timing of the data relative to the field number the software should read the **HANC** register, address 06H (shown below).

bit	7	6	5	4	3	2	1	0
	-	-	DFI2	DFI1	DFI0	-	-	ACTREN

DF2-0 Digital Field Identification, read only.
000 = Field 1, 011 = Field 4

The software should mask out all bits except bits 4 & 3. In NTSC mode, the field counter runs 0-3 for fields 1-4, this field number should be stored. It is preferable to transmit a character pair over the I^2C at the beginning of field 2 and 4 for line 21 field 1 encoding, and at the beginning of field 1 and 3 for line 21 field 2 encoding. This should ensure that the data is programmed before the relevant encoding field occurs. To prevent the current data from being overwritten, before the next byte pair is sent to the VP5311, the software should check that the field number has incremented by 2 from the previously read number.

Note that the non-printing characters used for control of the decoder are required to be sent twice i.e. on consecutive frames, this provides some error protection. If the software is interrupted before sending the second pair and therefore misses the next frame it is necessary to repeat the control character transmission from the start. This is not really a problem with printing characters as the VP5311 will send a 'null' character by default if it receives nothing. The 'null' character is ignored by the decoder.

Example of caption Coding

Information sent is shown with corresponding line data (2 bytes) in hex, without parity, below:

Caption Mode

EDM	**EDM**	**RDL**	**RDL**	*Information Sent*
142c	142c	1420	1420	*Hex data, no parity*

R1M	**R1M**	**RDL**	**RDL**	**HE**	**LL**	**Osp**	**fr**	**om**	**spG**	**PS**
1140	1140	1429	1429	4845	c4c4c	4f20	6672	6f6d	2047	5053

R3M	**R3M**	**RDL**	**RDL**	**VP**	**53**	**2sp**	**Cl**	**os**	**ed**	**spC**	**ap**	**ti**	**on**
1240	1240	1429	1429	5650	3533	3220	436c	6f73	6564	2043	6170	7469	6f6e

R5M	**R5M**	**RDL**	**RDL**	**fo**	**rsp**	**NT**	**SC**	**spo**	**nNU**	**spl**	**in**	**esp**	**21**
1540	1540	1429	1429	666f	7220	4e54	5343	206f	6e80	206c	696e	6520	3231

R14M	**R14M**	**RDL**	**RDL**	**Ha**	**ve**	**spa**	**spn**	**ic**	**esp**	**da**	**y!**
1440	1440	1429	1429	4861	7665	2061	206e	6963	6520	6461	7921

Text Mode (same message)

RT	RT	H E	LL	Osp	fr	om	spG	PS	N/L	N/L	*Information Sent*
142b	142b	4845	c4c4c	4f20	6672	6f6d	2047	5053	142d	142ad	*Hex data, no parity*

RT	RT	VP	53	11	spsp	Cl	os	ed	spC	ap	ti	on	N/L	N/L
142b	142b	5650	3533	3131	2020	436c	6f73	6564	2043	6170	7469	6f6e	142d	142d

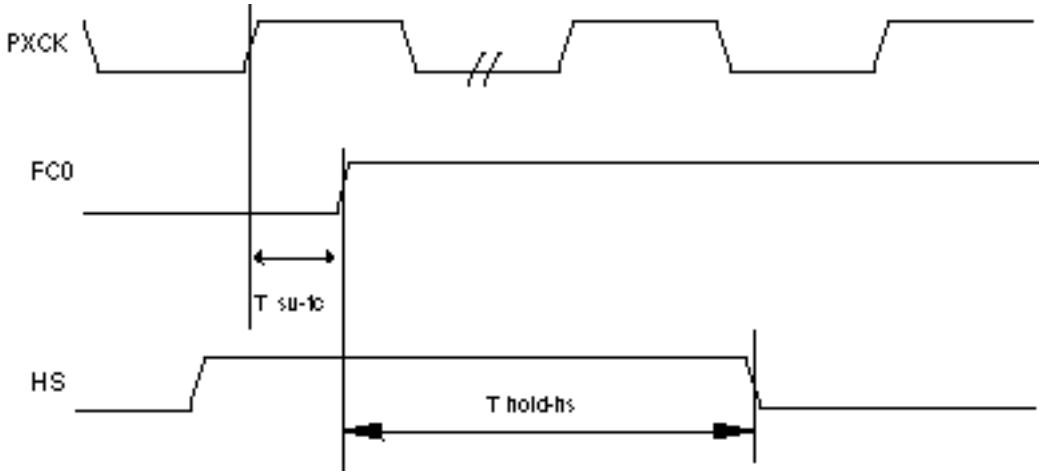
RT	RT	fo	rsp	N T	S C	sp o	n NU	sp l	in	esp	21	N/L	N/L
142b	142b	666f	7220	4e54	5343	206f	6e80	206c	696e	6520	3231	142d	142d

RT	RT	H a	ve	sp a	spn	ic	esp	da	y!	N/L	N/L	N/L	N/L
142b	142b	4861	7665	2061	206e	6963	6520	6461	7921	142d	142d	142d	142d

Abrieviations:

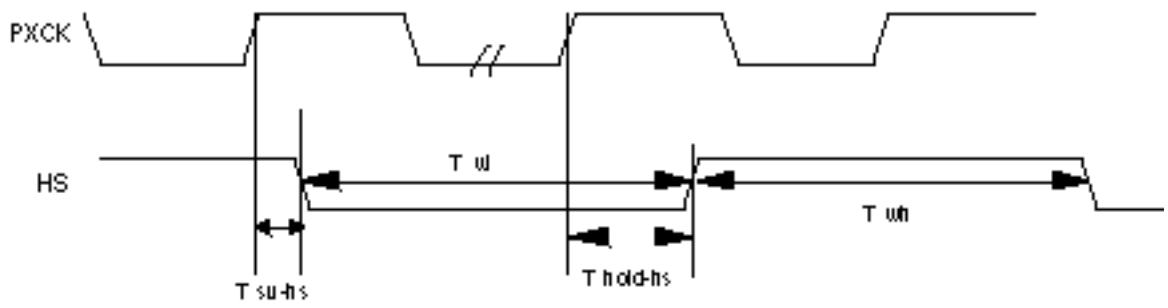
EDM Erase Non-Displayed Memory
RnM Row n Monochrome (Display position is row n, where n is replaced by a number)
RDL Resume Direct Loading
RT Resume Text
SC Show Caption
N/L New Line
NU NULL
sp SPACE

MASTER MODE TIMINGS



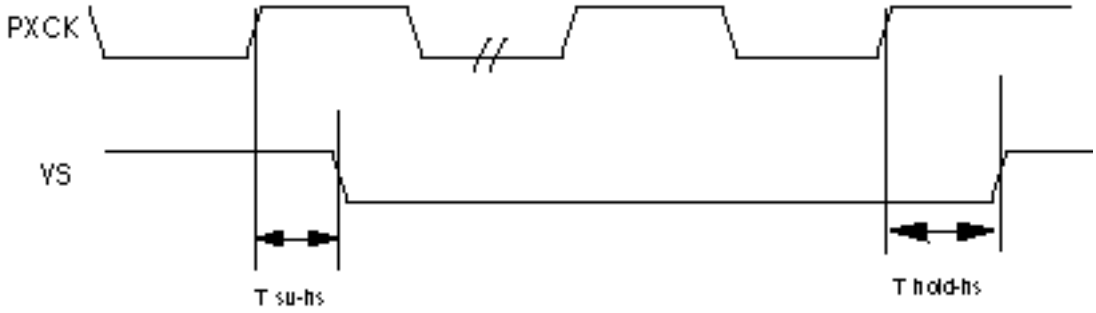
Tsu-fc = 15.01ns NTSC/PAL
Thold-hs = 40.70µs NTSC
= 41.74µs PAL

Fig.9 VP5311 Field Control Timings referenced to the pixel clock



Tsu-hs	=	14.94ns NTSC/PAL
Thold-hs	=	14.58 NTSC/PAL
Twl	=	4.74 µs NTSC/PAL
Twh	=	58.81µs NTSC
	=	59.26µs PAL

Fig.10 Horizontal Sync Timings



Tsu-vs	=	15.43ns NTSC/PAL
Thold-vs	=	15.06ns NTSC/PAL

Fig.11 Vertical Sync Timings

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Wiltshire SN2 2QW, United Kingdom.
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Fax: (01793) 518411

MITEL SEMICONDUCTOR
1500 Green Hills Road,
Scotts Valley, California 95066-4922
United States of America.
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